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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,979	12/31/2001	Toshio Miyamoto		6075

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EXAMINER	
CHAMBLISS, ALONZO	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,979	MIYAMOTO ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 49-74 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 49-74 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 31 December 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments, see request for reconsideration, filed 1/23/04, with respect to withdrawal of final rejection have been fully considered and are persuasive. The final rejection of claims 49-74 has been withdrawn. This action is made final.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 49, 51-58, 60, 62, 63, 65-70, 72, and 74 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Carpenter (U.S. 5,541,448).

With the respect Claims 49, 57, 58, and 63, Carpenter discloses providing first semiconductor devices 58 each having a DRAM semiconductor chip and protruded terminals arranged over the DRAM semiconductor chip. A second semiconductor device has a package body, a nonvolatile memory semiconductor chip (i.e. EPPROM) sealed in the package body and outer leads protruding outwardly from a side surface of the package body. As stated in col. 1 lines 16-24 and col. 4 lines 16-23, any one of the electronic devices can be EPROMs or DRAMs. A module board having first terminals and second terminals; and mounting the first semiconductor devices 58 and the second semiconductor device 60 on the module board, wherein the mounting step is performed such that the protruded terminals of the first semiconductor devices 58 are arranged

and between the DRAM semiconductor chips of the first semiconductor devices and the module board 52 in a sectional view and arranged at the inside of the DRAM semiconductor chips of the first semiconductor devices in a plan view, and the protruded terminals of each of the first semiconductor devices are soldered to the first terminals of the module board 15 and such that the outer leads of the second semiconductor device are soldered to the second terminals of the module board 52 at the outside of the package body in the plan view. Each of the protruding terminals is soldered to terminals of the board 52 (see col. 4 lines 3-23; Figs. 5 and 6).

With respect to Claims 51 and 65, Carpenter teaches wherein each of the outer leads of the second semiconductor device 60 is exposed to the air between the package body and a portion of the outer leads that connect to the second terminals (see Figs. 5-7).

With respect to Claims 52 and 66, Carpenter teaches wherein each of the DRAM semiconductor chips 58 of the first semiconductor devices has a main surface and bonding electrodes on the main surface, and wherein the protruded terminals are arranged over the main surface and electrically connected to the bonding electrodes (see col. 4 lines 5-15; Figs. 6).

With respect to Claims 53 and 67, Carpenter teaches wherein the mounting step is performed so that the main surfaces of the DRAM semiconductor chips of the first semiconductor devices face the module board (see Fig. 6).

With respect to Claims 54 and 68, Carpenter teaches wherein in surface of the DRAM semiconductor the mounting step, the back chip of each of the first semiconductor devices 58 are exposed (see Fig. 5).

With respect to Claims 55 and 69, Carpenter teaches sealing a space between each of the first semiconductor devices 58 and the module board 52 with resin 76 (see col. 4 lines 60-67; Fig. 6).

With respect to Claims 56 and 70, Miyazaki discloses wherein all protruded terminals of each of the first semiconductor devices 58 are arranged between the corresponding semiconductor chip of the corresponding first semiconductor device and the module board 52 (see Fig. 6).

With respect to Claims 60 and 72, Carpenter disclose in col. 5 lines 3 – 10 that the components (i.e. devices 58 and 60) can be arranged differently without requiring modifications in the case 44. Thus, Carpenter in a different arrangement includes a wherein the number of first devices 58 is larger than that of the second device on the module board.

With respect to Claims 62 and 74, Carpenter disclose in the background of the invention that integrated circuits solder attached to connection spots (i.e. terminals) on a printed wiring board (see col. 1 lines 59-67). Thus, the outer leads of the second devices 60 are soldered to the second terminals.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 50, 59, 61, 64, 71, and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter (U.S. 5,541,448) as applied to claims 49 and 63 above, and further in view of Elenius et al. (U.S. 6,287,893).

With respect to Claims 50 and 64, one skilled in the art would readily recognize having protruding terminals arranged in rows and columns between each of the DRAM semiconductor chips of the first semiconductor devices and the module board, since the arrangement provides a multiplicity of electrical connection that would increase the signals between the devices and the board. Therefore, it would have been obvious to incorporate terminal arranged in rows and columns between each of the DRAM semiconductor chips of the first semiconductor devices and the module board of

Carpenter, since the arrangement provides a multiplicity of electrical connection that would increase the signals between the devices and the board.

With respect to Claims 59 and 71, one skilled in the art would readily recognize to simultaneously soldering the first semiconductor devices and the second semiconductor device to mount them on the module board after the step of arranging the first semiconductor devices and the second semiconductor device on the module board after the step of arranging the first and second devices, since simultaneously soldering a plurality of devices would save time during manufacturing which would reduce the cost of the memory module. Therefore, it would have been obvious to incorporate the simultaneous soldering of the first and second devices of Miyazaki, since simultaneously soldering a plurality of devices would save time during manufacturing which would reduce the cost of the memory module.

With respect to Claims 61 and 73, Carpenter discloses wherein the DRAM chips 58 of the first devices each have bonding electrodes attached to protruding terminals (see col. 4 lines 5-15; Fig 6). Carpenter fails to disclose wherein a minimum pitch of the bonding electrodes is larger than a minimum pitch of the protruded terminals of the respective first device. However, Elenius discloses wherein a minimum pitch of the bonding electrodes 18, 26 is larger than a minimum pitch of the protruded terminals 28 of the respective first device (see Figs. 1 and 2). Thus, Carpenter and Elenius have substantially the same environment of flip chip integrated circuit. Therefore, it would have been obvious to incorporate a pitch of the electrodes being greater than the pitch of the protruded terminals with the process of Carpenter, since the pitch would allow the

protruding terminals to have a larger diameter without risking the terminals from abutting each other while creating a larger electrical interface with an external device as taught by Elenius.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Alonzo Chambliss
Patent Examiner
Art Unit 2827

AC/February 10, 2004